UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,940,875 B2
APPLICATION NO. : 10/643792
DATED : September 6, 2005
INVENTOR(S) : Mesecher et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete the title page and substitute therefor the attached title page.

ON THE TITLE PAGE

At Item (57), line 1, before the word "for", delete "reciever" and insert therefor --receiver--.

IN THE DRAWINGS

Please replace Figures 2-5 and 11 with replacement Figures 2-5 and 11 attached hereto.

IN THE SPECIFICATION

At column 2, line 13, after the word "a", delete "B-CDMATM" and insert therefor --B-CDMA™--.

At column 2, line 40, after the word "present", delete "inventor" and insert therefor --invention--.

At column 5, line 53, after the word "mixer", delete "122" and insert therefor --110--.

At column 5, line 67, equation 2, delete " $m=\sqrt{(I^{2+Q^2})}$ " and insert therefor -- $m=\sqrt{I^2+Q^2}$ --.

At column 9, line 55, after the word "The", delete "anaysis" and insert therefor --analysis--.

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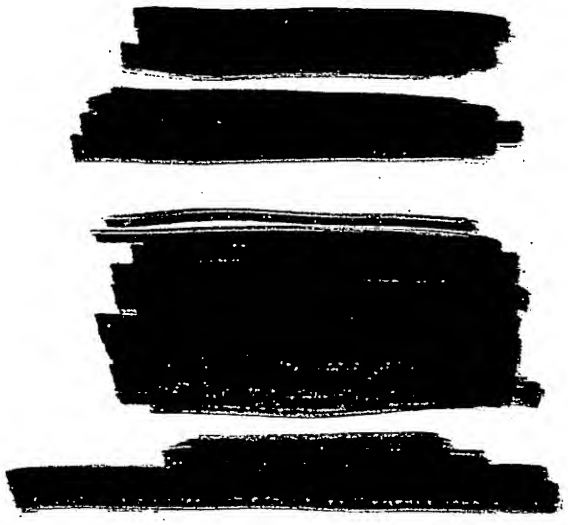
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

In claim 24, at column 12, line 42, after the word "response", insert --to--.



US006940875B2

(12) **United States Patent**
Mesecher et al.

(10) **Patent No.: US 6,940,875 B2**
(45) **Date of Patent: *Sep. 6, 2005**

(54) **CONTINUOUSLY ADJUSTED-BANDWIDTH DISCRETE-TIME PHASE-LOCKED LOOP**

(75) Inventors: **David K. Mesecher**, Huntington Station, NY (US); **Rui Yang**, Greenlawn, NY (US); **Ramon Cerda**, West Babylon, NY (US)

(73) Assignee: **InterDigital Technology Corporation**, Wilmington, DE (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/643,792**

(22) Filed: **Aug. 19, 2003**

(65) **Prior Publication Data**

US 2004/0032842 A1 Feb. 19, 2004

Related U.S. Application Data

(63) Continuation of application No. 09/558,686, filed on Apr. 24, 2000, now Pat. No. 6,608,826, which is a continuation of application No. 08/871,109, filed on Jun. 9, 1997, now Pat. No. 6,055,231.

(60) Provisional application No. 60/037,914, filed on Mar. 12, 1997.

(51) **Int. Cl.**[7] **H04J 3/06**

(52) **U.S. Cl.** **370/516**; 370/252; 370/342; 375/136; 375/294

(58) **Field of Search** 370/252, 328, 370/329, 335, 342, 441, 463, 516, 330, 320; 375/136, 147, 294, 344, 206, 200, 150, 222; 379/406.08

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,983,501	A	9/1976	Lindstrum	329/307
4,243,941	A	1/1981	Zdunek	329/309
4,354,277	A	10/1982	Crackel et al.	455/259
4,513,429	A	4/1985	Roeder	375/376
4,630,283	A	12/1986	Schiff	375/143
5,029,180	A	7/1991	Cowart	375/141
5,049,830	A	9/1991	Yoshida	329/306
5,065,107	A	11/1991	Kumar et al.	329/308
5,101,416	A	3/1992	Fenton et al.	375/150
5,142,246	A	8/1992	Petersson	331/11
5,166,952	A	11/1992	Omura et al.	375/149
5,175,729	A	12/1992	Borras et al.	370/345

(Continued)

FOREIGN PATENT DOCUMENTS

WO 9620540 7/1996

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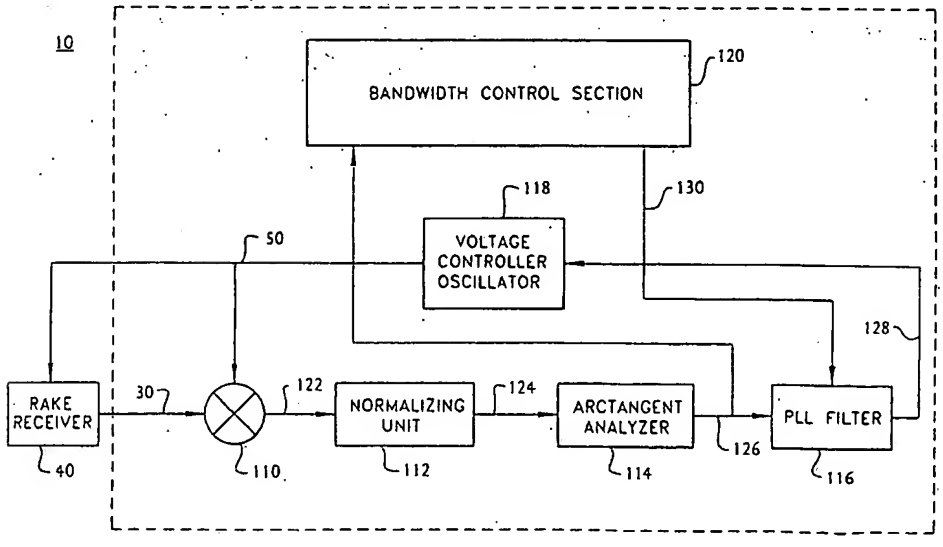
(74) *Attorney, Agent, or Firm*—Volpe and Koenig, P.C.

(57) **ABSTRACT**

A receiver for receiving a CDMA communication signal that is wirelessly transmitted includes a system for correcting phase errors in an information signal which has been transmitted. The correction system comprises circuitry for generating a mixing signal and for combining the mixing signal with said information signal to produce a correction signal. An analyzer analyzes the phase of said correction signal and generates an error signal based on the deviation of the analyzed phase from a reference phase. A bandwidth controller which recursively adjusts the phase of the correction signal such that the phase of said correction signal is substantially equal to said reference phase. The bandwidth controller then selects a bandwidth within an adjustable range based on the correction signal, estimates an offset by interrogating the error signal, and modifies said correction signal by the offset.

25 Claims, 14 Drawing Sheets



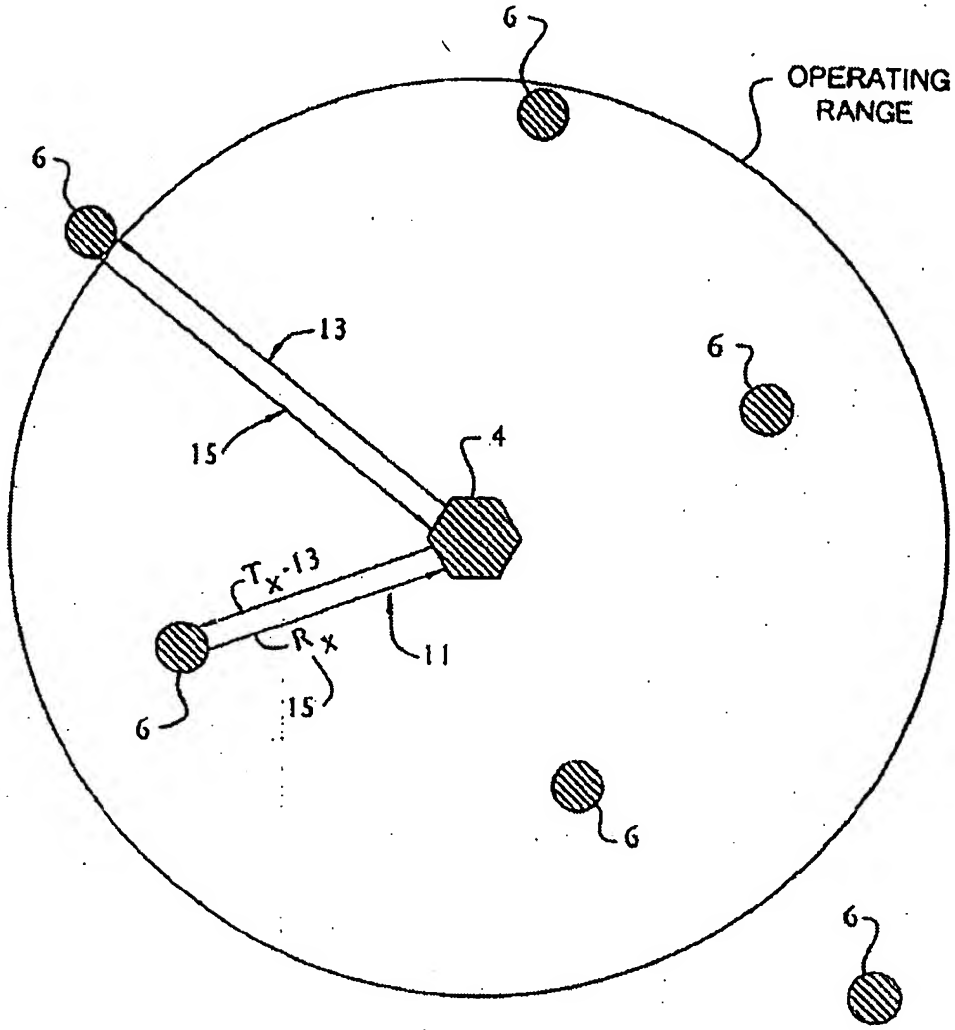


FIG. 2

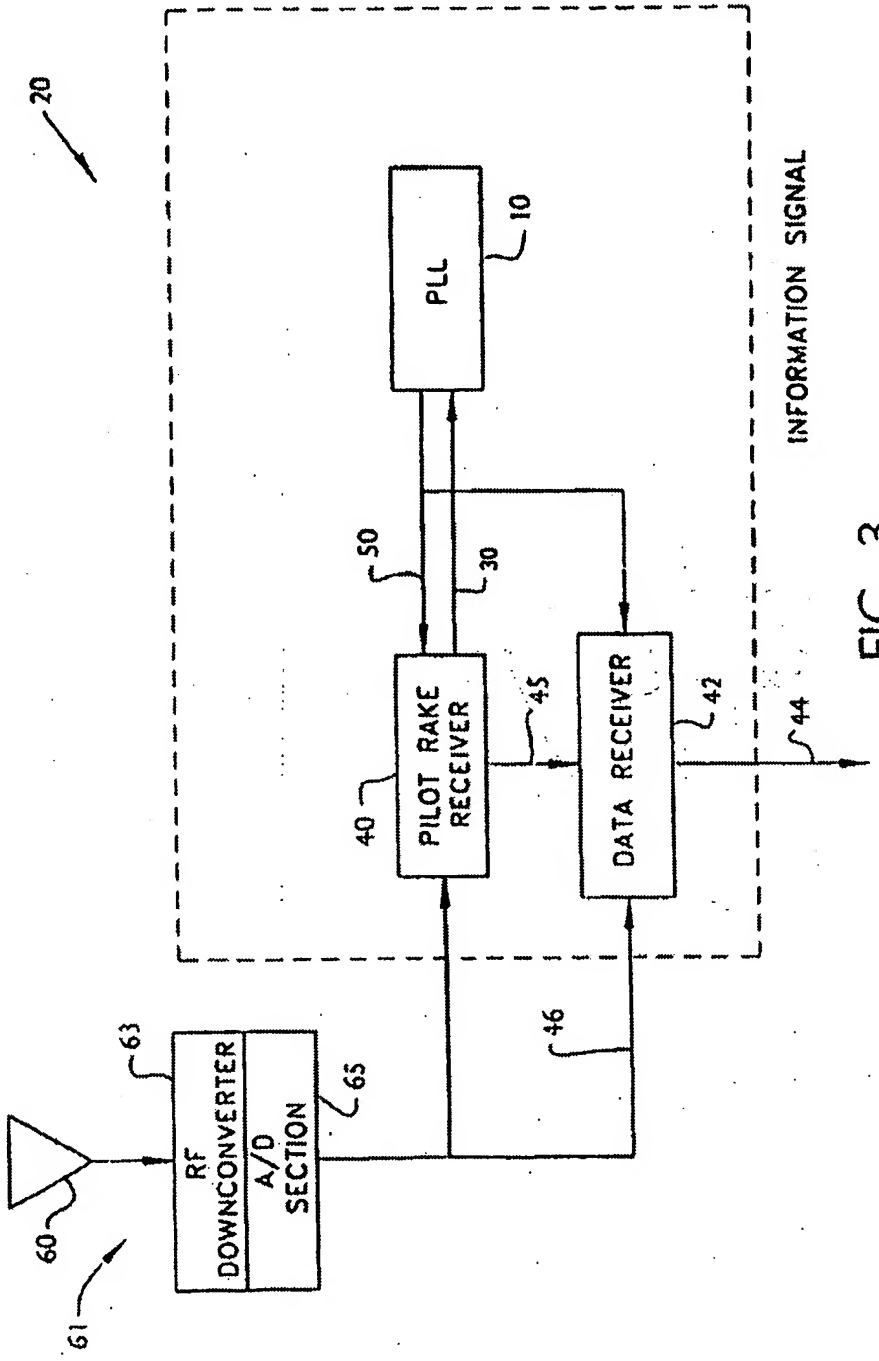

20
PLL
10
INFORMATION SIGNAL
50
30
PILOT RAKE RECEIVER
40
45
DATA RECEIVER
42
44
46
63
RF DOWNCONVERTER
A/D SECTION
65
60
61

FIG. 3

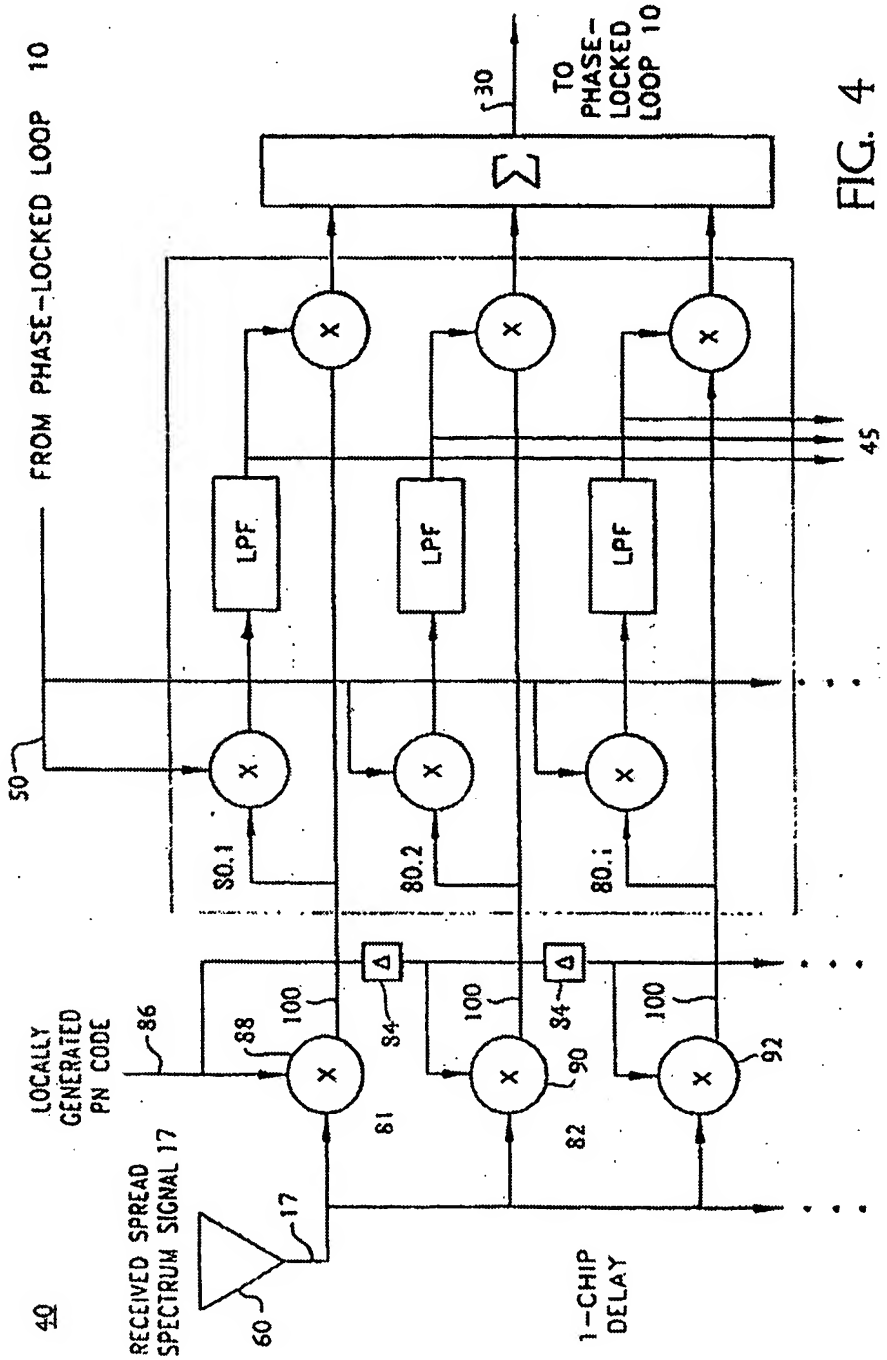

FROM PHASE-LOCKED LOOP 10
TO PHASE-LOCKED LOOP 10
30
LPF
LPF
LPF
45
50
80.1
80.2
80.i
LOCALLY GENERATED PN CODE
86
88
100
84
90
92
81
82
RECEIVED SPREAD SPECTRUM SIGNAL 17
17
60
40
1-CHIP DELAY

FIG. 4

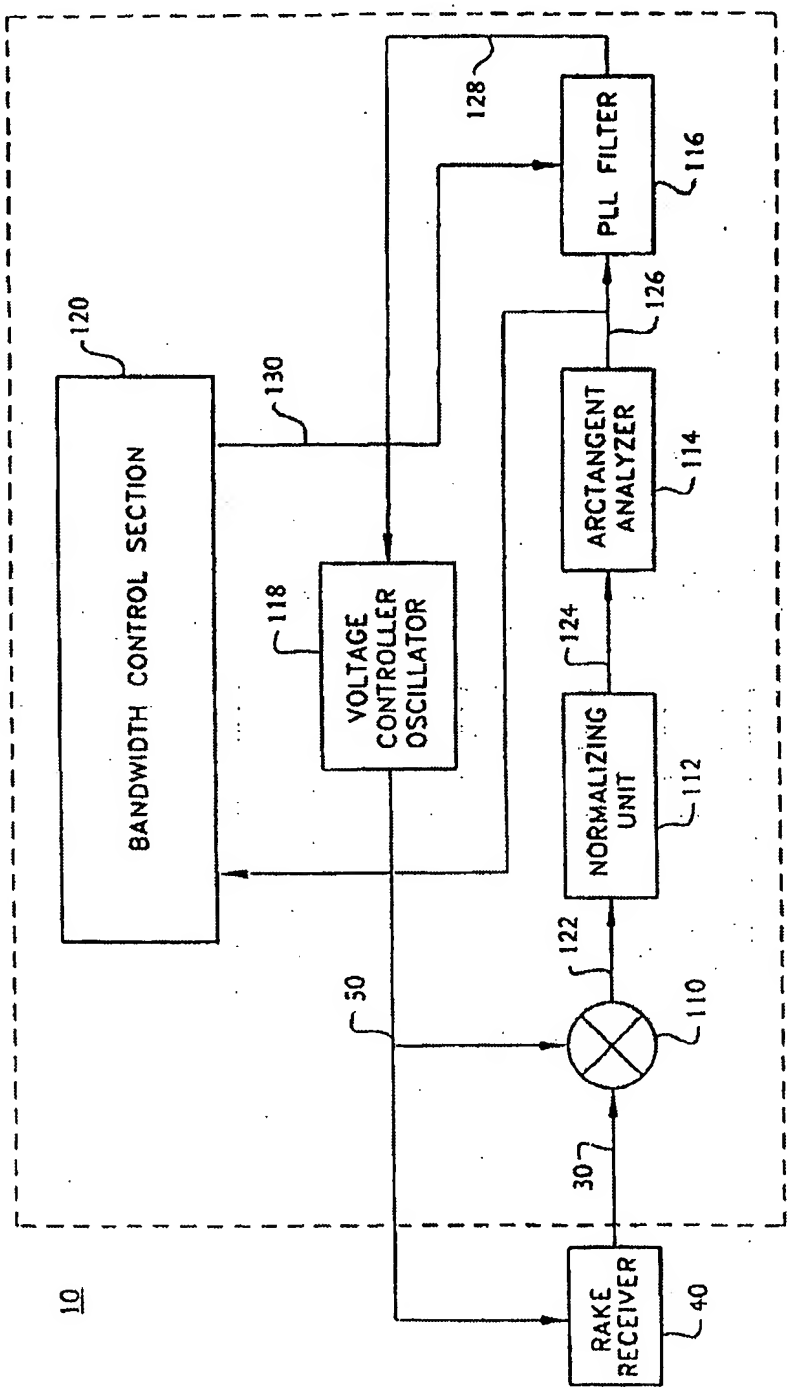

10
BANDWIDTH CONTROL SECTION
120
130
VOLTAGE CONTROLLER OSCILLATOR
118
128
PLL FILTER
116
126
ARCTANGENT ANALYZER
114
124
NORMALIZING UNIT
112
122
50
110
30
RAKE RECEIVER
40

FIG. 5

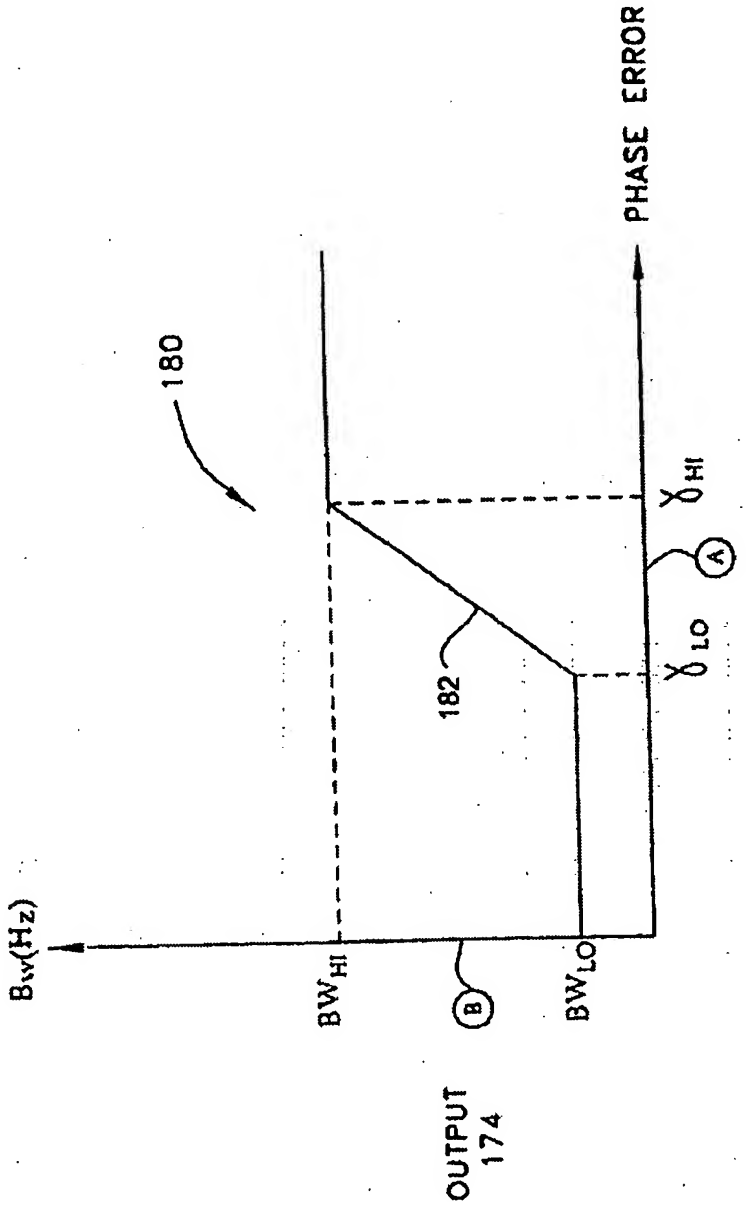

PHASE ERROR
180
γ_{HI}
A
γ_{LO}
182
INPUT 172
B_W(Hz)
BW_{HI}
B
BW_{LO}
OUTPUT 174

FIG. 11